Memory Access Protocols:
Certified Data-Race Freedom for GPU Kernels

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Joint work with

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Today's talk

Impact (Part 1)

- why GPUs
- what makes static analysis of GPU programs unique
- a static DRF analysis for GPU programs
- more robust, more scalable in largest comparative study of its kind

Theoretical contributions (Part 2)

- a novel analysis of data-race freedom
- a formalization of such analysis using a proof assistant

Published works

- Checking Data-Race Freedom of GPU Kernels, Compositionally (CAV'21)
- Memory Access Protocols: Certified Data-Race Freedom for GPU Kernels (FMSD'23)
Motivation
Why do GPUs matter?

GPUs are everywhere
GPUs are a computing cornerstone of scientific advancement
## GPUs in High Performance Computing (HPC)

Power 8 out of 10 of the Top 10 super computers

<table>
<thead>
<tr>
<th>Name</th>
<th>GPU</th>
</tr>
</thead>
<tbody>
<tr>
<td>1 Supercomputer Fugaku</td>
<td>☐</td>
</tr>
<tr>
<td>2 Summit</td>
<td>✓</td>
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<tr>
<td>3 Sierra</td>
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<td>4 Sunway TaihuLight</td>
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<td>5 Selene</td>
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<td>6 Tianhe-2A</td>
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<td>7 JUWELS Booster Module</td>
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<td>8 HPC5</td>
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<td>9 Frontera</td>
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<tr>
<td>10 Dammam-7</td>
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</table>


*Credit: Carlos Jones/ORNL*
Topical perspectives

GPU-accelerated molecular modeling coming of age

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A B S T R A C T

Graphics processing units (GPUs) have traditionally been used in molecular modeling solely for visualization of molecular structures and animation of trajectories resulting from molecular dynamics simulations. Modern GPUs have evolved into fully programmable, massively parallel co-processors that can now be exploited to accelerate many scientific computations, typically providing about one order of magnitude speedup over CPU code and in special cases providing speedups of two orders of magnitude. This paper surveys the development of molecular modeling algorithms that leverage GPU computing, the advances already made and remaining issues to be resolved, and the continuing evolution of GPU technology that promises to become even more useful to molecular modeling. Hardware acceleration with commodity GPUs is expected to benefit the overall computational biology community by bringing teraflops performance to desktop workstations and in some cases potentially changing what were formerly batch-mode computational jobs into interactive tasks.

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GPU computing for systems biology

Lorenzo Dematté and Davide Prandi

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Abstract
The development of detailed, coherent, models of complex biological systems is recognized as a key requirement for integrating the increasing amount of experimental data. In addition, in-silico simulation of bio-chemical models provides an easy way to test different experimental conditions, helping in the discovery of the dynamics that regulate biological systems. However, the computational power required by these simulations often exceeds that available on common desktop computers and thus expensive high performance computing solutions are required. An emerging alternative is represented by general-purpose scientific computing on graphics processing units (GPGPU), which offers the power of a small computer cluster at a cost of ~$400. Computing with a GPU requires the development of specific algorithms, since the programming paradigm substantially differs from traditional CPU-based computing. In this paper, we review some recent efforts in exploiting the processing power of GPUs for the simulation of biological systems.

Keywords: systems biology; simulation; agent-based modelling; cellular automata; GPGPU; CUDA

doi: 10.1093/bib/bbq006
GPUs power the AI revolution
Autoware.AI

Autoware.AI is the world’s first "All-in-One" open-source software for autonomous driving technology.

22 code results in Autoware-AI/core_perception

- nct_gpu/src/MatrixDevice.cu
  - Cuda  Last indexed on Oct 15, 2020

- nct_gpu/src/SymmetricEigenSolver.cu
  - Cuda  Last indexed on Oct 15, 2020

- vision_darknet_detect/darknet/src/dropout_layer_kernels.cu
  - Cuda  Last indexed on Oct 15, 2020

- vision_darknet_detect/darknet/src/col2im_kernels.cu
  - Cuda  Last indexed on Oct 15, 2020
Why we should care about static verification of GPU programs?
GPU programming, a primer

① High-level of parallelism at a reduced cost
(faster processing, lower cost, reduced power consumption)

② Techniques designed for CPUs do not work for GPUs
(hardware assumptions differ: memory available, execution model)

③ GPUs are difficult to program and debug
GPU programming is difficult

- high degree of parallelism (up to tens of thousand of threads)
- high degree of concurrency (up to 1,024 threads accessing the same array)
- **unconstrained** access to a shared memory (no locks)
- thousands of threads indexing disjoint portions of arrays
- devices are memory constrained *(affects debugging techniques)*
for (int r = 0; r < N; r++) {
    for (int i = 0; i<TILE_DIM; i+=BLOCK_ROWS) {
        tile [ tid .y+i ][ tid .x ] = idata [ index_in+i*width ];
    }
    __syncthreads();
    for (int j = 0; j<TILE_DIM; j+=BLOCK_ROWS) {
        odata [ index_out+j*height ] = tile [ tid .x ][ tid .y+j ];
    }
}

Source:
- Optimizing matrix transpose in CUDA. NVIDIA CUDA SDK Application Note 18 (2009)

Also in:
- Padding free bank conflict resolution for CUDA-based matrix transpose algorithm. DOI: 10.1109/SNPD.2014.6888709
for (int r = 0; r < N; r++) {
    for (int i = 0; i<TILE_DIM; i+=BLOCK_ROWS)
        tile [tid.y+i][tid.x] = idata [index_in+i*width];
    syncthreads();
    for (int j = 0; j<TILE_DIM; j+=BLOCK_ROWS)
        odata[index_out+j*height] = tile [tid.x][tid.y+j];
}
for (int r = 0; r < N; r++) {
    for (int i = 0; i<TILE_DIM; i+=BLOCK_ROWS)
        { tile [0][1+i] = idata [index_in+i*width]; }
    syncthreads();
    for (int j = 0; j<TILE_DIM; j+=BLOCK_ROWS)
        { odata[index_out+j*height] = tile [1][0+j]; }
}

for (int r = 0; r < N; r++) {
    for (int i = 0; i<TILE_DIM; i+=BLOCK_ROWS)
        { tile [1][0+i] = idata [index_in+i*width]; }
    syncthreads();
    for (int j = 0; j<TILE_DIM; j+=BLOCK_ROWS)
        { odata[index_out+j*height] = tile [0][1+j]; }
}
GPU data-races

Data-race

- Two threads accessing the same array index concurrently
- At least one thread writing

Data-Race Freedom (DRF) analysis

Show that for all possible inputs and executions a program is absent of data-races.

A trivial data-race example (every thread writes to position 0)

\[
A[0] = 1;
\]
GPU program example

```c
for (int r = 0; r < N; r++) {
    for (int i = 0; i<TILE_DIM; i+=BLOCK_ROWS) {
        tile [ tid .y+i ][ tid .x ] = idata [index_in+i*width];
    }
    __syncthreads();
    for (int j = 0; j<TILE_DIM; j+=BLOCK_ROWS) {
        odata[index_out+j*height] = tile [ tid .x][ tid .y+j ];
    }
}
```

Exhibits a data-race: the code after `__syncthreads()` of iteration $i + 1$ runs concurrently with the code before `__syncthreads()` of iteration $i$.

- Outer loops is used to measure the benefit of an optimization
- Data-race **corrupts** the data in the array and affects the time measurements
Contributions
Contributions

Impact (Part 1)

- a static DRF analysis for GPU programs
- more robust, more scalable in largest comparative study of its kind

Theoretical contributions (Part 2)

- a novel analysis of data-race freedom
- a formalization of such analysis using a proof assistant
Lowest false-positive rate

- Dataset of 227 data-race free real-world kernels
- Can verify 41% more kernels than others

**Faial** *(our tool)*

- C: 95.6% (217)
- F: 4.0% (9)
- U: 0.4% (1)
- T: 0.0% (0)

**GPUVerify**

- C: 68.3% (155)
- F: 22.0% (50)
- U: 0.4% (1)
- T: 9.3% (21)

**PUG**

- C: 35.2% (80)
- F: 2.6% (6)
- U: 62.1% (141)
- T: 0.0% (0)
Best compromise time/memory
Highest scalability

- Vary the number of constructs from 1 to 50 (250 kernels in total)
- Out of 5 tools, the only that **scales linearly** (time) (PUG, GPUVerify, GKlee, SESA)
Limitations of our analysis

- Cannot handle more than 13 nested synchronized loops
- 3rd out of 5 tools
- We found a maximum nesting level of 3 in our experiments
Demo
Theoretical contributions

- Property: **DRF analysis (in green) is proved sound & complete** (Theorem 1)
- Technique: A behavioral type (syntax+semantics)
- Artifact: Mechanized proofs using the Coq proof assistant (18,000 LOC)
Remainder of the talk

• Present our main result
• Introduce a motivating example
• Detail our analysis
  1. Align protocols
  2. Split protocols
  3. Sequentialize protocols
Main result

Let $\text{safe}(H)$ mean that $H$ is data-race free.

**Theorem 1.** If $p \downarrow H_1$ and $\text{seq}(\text{split}(\text{align}(p))) \downarrow H_2$, then $\text{safe}(H_1)$ if and only if $\text{safe}(H_2)$.

- Analysis steps seq, split, align are sound and complete, wrt the DRF property
- The over-approximations happen before MAP is created (protocol inference)
- We further show that the set of concurrent accesses is preserved (more general)
Theorem 1. If \( p \downarrow H_1 \) and \( \text{seq}(\text{split}(\text{align}(p))) \downarrow H_2 \), then \( \text{safe}(H_1) \) if and only if \( \text{safe}(H_2) \).

Fig. 9: Overview of the key lemmas used to establish Theorem 1.
Simplified running example

- A CUDA example, which simplifies our initial example
- Exhibits the same root cause (data-race)

```c
1  for (int r = 0; r < N; r++) {
2      for (int i = 0; i < M; i++)
3      { tile[tid] = ...; }
4      syncthreads();
5  for (int j = 0; j < M; j++)
6      { ... = tile[tid+j]; }
```
\[
\forall r, j_1, i_1, j_2, i_2 : 1 \leq r < N \land 0 \leq j_1 < M \land 0 \leq i_1 < M \land 0 \leq j_2 < M \land 0 \leq i_2 < M
\]
\[
\implies \{ rd[t_1 + j_1] \} \cup \{ wr[t_1] \} \quad DRF \ with? \quad \{ rd[t_2 + j_2] \} \cup \{ wr[t_2] \}
\]
Memory access protocols

- Behavioral types for SIMT/SPMD that capture memory accesses
- One type per array. Capture: accesses, synchronization, structured loops
- Distinguish between synchronized/unsynchronized loops

**Ongoing work (inference):** Provable GPU Data-Races in Static Race Detection [PLACES’22]
A racy protocol

```c
for^S r in 0..N {
    for^U i in 0..M { wr[tid] }
    sync;
    for^U j in 0..M { rd[tid + j] }
}
```

data-race

```c
// r = 0
for^U j in 0..M
    rd[tid+j];
// r = 1
for^U i in 0..M
    wr[tid]
```

// for (int j = 0; j<M; j++)
//    _ = tile[tid+i];
// for (int i = 0; i<M; i++)
//    tile[tid] = _;

How do we solve the core problem?

Proving data-race-freedom in the unsynchronized fragment
A data-race in the unsynchronized fragment

**Data-race:** \( t_1 = 0, t_2 = 1, j_1 = 1, M > 1 \): \( \text{rd}[1] \) and \( \text{wr}[1] \).

```plaintext
// r = 0
for\(^{y} j \) in 0..M
    \{ \text{rd}[\text{tid}+j] \}; // for (\text{int} j = 0; j<M; j++)
// r = 1
for\(^{y} i \) in 0..M
    \{ \text{wr}[\text{tid}] \}; // for (\text{int} i = 0; i<M; i++)
```

**Assumptions**

- No synchronizations possible
- **Data-race:** given \( t_1 \neq t_2 \), index of \( t_1 \) equals index of \( t_2 \) and at least one is a write.

---

\[ \forall j_1, i_1, j_2, i_2 : 0 \leq j_1 < M \land 0 \leq i_1 < M \land 0 \leq j_2 < M \land 0 \leq i_2 < M \implies \]
\[ \{ \text{rd}[t_1 + j_1] \} \cup \{ \text{wr}[t_1] \} \quad \text{DRF with?} \quad \{ \text{rd}[t_2 + j_2] \} \cup \{ \text{wr}[t_2] \} \]

\[ \iff \text{index}(a_1) = \text{index}(a_4) \lor \text{index}(a_2) = \text{index}(a_3) \lor \text{index}(a_2) = \text{index}(a_4) \]
\[ \iff t_1 + j_1 = t_2 \lor t_1 = t_2 + j_2 \lor t_1 = t_2 \]
Sequentializing protocols (step 3)

- **Idea:** represent the interleaving of any two threads (instead of all available threads) (FSE’10)
  - Each variable is duplicated per thread (thread-local view)
  - Interpret loops as $\forall$-binders (FSE’10)
- **Key insight:** Data-races are isolated on pairs of threads (not a transitive)

(FSE’10) Scalable SMT-Based Verification of GPU Kernel Functions. Guodong Li and Ganesh Gopalakrishnan.
Sequentializing protocols

Source syntax

\[ \mathcal{U} \ni u ::= \text{skip} \mid o[n] \mid u \; ; \; u \mid \text{if } b \{u\} \text{ else } \{u\} \mid \text{for}^u x \in n..m \{u\} \]

Target syntax

\[ \mathcal{L} \ni h ::= \text{skip} \mid n:o[m] \mid h \; ; \; h \mid \text{if } b \{h\} \text{ else } \{h\} \mid \text{var } x \text{ in } n..m; \; h \]

Tracing

\[
\begin{align*}
\text{trace}(\text{skip}) &= \text{skip} & \text{trace}(o[n]) &= \text{id}:o[n] \\
\text{trace}(u_1 \; ; \; u_2) &= \text{trace}(u_1) \; ; \; \text{trace}(u_2) \\
\text{trace}(\text{if } b \{u_1\} \text{ else } \{u_2\}) &= \text{if } b \{\text{trace}(u_1)\} \text{ else } \{\text{trace}(u_2)\} \\
\text{trace}(\text{for}^u x \in n..m \{u\}) &= \text{var } x \text{ in } n..m; \; \text{trace}(u)
\end{align*}
\]
Sequentializing protocols

Sequencing

\[ h_1 = \text{trace}(u)[\text{tid} := t_1] \quad h_2 = \text{trace}(u)[\text{tid} := t_2] \]

\[ \text{seq}(u) = \text{var } t_1 \text{ in } 1..|\mathbb{T}|; \text{ var } t_2 \text{ in } 0..t_1; \quad h_1 ; h_2 \]

\[ \text{seq}(\text{var } x \text{ in } n..m; \ c) = \text{var } x \text{ in } n..m; \quad \text{seq}(c) \]

\[ \text{seq}([c_1, \ldots, c_n]) = [\text{seq}(c_1), \ldots, \text{seq}(c_n)] \]

Results

**Lemma 17.** If \( \phi \subseteq^h \text{seq}(c) \), then \( \phi \subseteq^c c \).

**Lemma 18.** Let \( \phi = (\alpha_1, \alpha_2) \). If \( \text{owner}(\alpha_1) \neq \text{owner}(\alpha_2) \) and \( \phi \subseteq^c c \), then \( \phi \subseteq^h \text{seq}(c) \).
How do we get to unsychronized protocols?
Aligning protocols

(step 1)
Aligning protocols (step 1)

- We define a notion of **aligned** protocols, where accesses do not "leak" across iterations.
- We show that all protocols can be aligned (modulo notion of well-formedness).
- **Intuition:** unfold loop and rearrange accesses.
- **Insight:** protocols have no local state; ordering only matter wrt synch.
Aligning protocols

Source: well-formed protocols

$$\mathcal{W} \ni p ::= u \; ; \; \text{sync} \; | \; p \; ; \; p \; | \; u \; ; \; \text{for}^S \; x \in n..m \; \{p \; ; \; u\}$$

Target: aligned protocols

$$\mathcal{A} \ni a ::= u \; ; \; \text{sync} \; | \; a \; ; \; a \; | \; a \; ; \; \text{for}^S \; x \in n..m \; \{a\}$$
Aligning protocols

\[ \gamma \text{-ACC} \]
\[ \phi \subseteq^w u \]
\[ \phi \subseteq^w u ; \text{ sync} \]

\[ \gamma \text{-SEQ-L} \]
\[ \phi \subseteq^w p \]
\[ \phi \subseteq^w p ; q \]

\[ \gamma \text{-SEQ-R} \]
\[ \phi \subseteq^w p \]
\[ \phi \subseteq^w p ; q \]

\[ \gamma \text{-SEQ-B} \]
\[ \alpha_1 \in^w \text{lst}(p) \]
\[ \alpha_2 \in^w \text{fst}(q) \]
\[ (\alpha_1, \alpha_2) \subseteq^w p ; q \]

\[ \subseteq^w \text{-FOR-1} \]
\[ \phi \subseteq^u u_1 \]
\[ \phi \subseteq^w u_1 ; \text{ for}^S \ x \in n..m \ \{p ; u_2\} \]

\[ \subseteq^w \text{-FOR-2} \]
\[ \alpha_1 \in^u u_1 \]
\[ \alpha_2 \in^w \text{fst}(p[x := n]) \]
\[ (\alpha_1, \alpha_2) \subseteq^w u_1 ; \text{ for}^S \ x \in n..m \ \{p ; u_2\} \]
Aligning protocols

\[ \subseteq^{w}_{-FOR-3} \]
\[ \begin{array}{c}
\forall n \downarrow j \quad m \downarrow k \\
\exists i : j \leq i < k \\
\phi \subseteq^{w} p[x := i]
\end{array} \]
\[ \phi \subseteq^{w} u_1 ; \text{for}^{s} x \in n..m \{p ; u_2\} \]

\[ \subseteq^{w}_{-FOR-4} \]
\[ \begin{array}{c}
\forall n \downarrow j \quad m \downarrow k \\
\exists i : j \leq i < k \\
\phi \subseteq^{w} u_2[x := i]
\end{array} \]
\[ \phi \subseteq^{w} u_1 ; \text{for}^{s} x \in n..m \{p ; u_2\} \]

\[ \subseteq^{w}_{-FOR-5} \]
\[ \begin{array}{c}
\forall n \downarrow j \quad m \downarrow k \\
\exists i : j \leq i < k \\
\alpha_1 \in^{w} \text{lst}(p[x := i]) \\
\alpha_2 \in^{v} u_2[x := i]
\end{array} \]
\[ (\alpha_1, \alpha_2) \subseteq^{w} u_1 ; \text{for}^{s} x \in n..m \{p ; u_2\} \]

\[ \subseteq^{w}_{-FOR-6} \]
\[ \begin{array}{c}
\forall n \downarrow j \quad m \downarrow k \\
\exists i : j \leq i < k \\
\alpha_1 \in^{v} u_2[x := i] \\
\alpha_2 \in^{w} \text{fst}(q[x := i + 1])
\end{array} \]
\[ (\alpha_1, \alpha_2) \subseteq^{w} u_1 ; \text{for}^{s} x \in n..m \{p ; u_2\} \]

\[ \subseteq^{w}_{-FOR-7} \]
\[ \begin{array}{c}
\forall n \downarrow j \quad m \downarrow k \\
\exists i : j \leq i < k \\
\alpha_1 \in^{w} \text{lst}(q[x := i]) \\
\alpha_2 \in^{w} \text{fst}(q[x := i + 1])
\end{array} \]
\[ (\alpha_1, \alpha_2) \subseteq^{w} u_1 ; \text{for}^{s} x \in n..m \{p ; u_2\} \]
Splitting protocols

(step 3)
Splitting protocols

\[ \forall r, j_1, i_1, j_2, i_2: \ 1 \leq r < N \land 0 \leq j_1 < M \land 0 \leq i_1 < M \land 0 \leq j_2 < M \land 0 \leq i_2 < M \]

\[ \Rightarrow \{ \text{rd}[t_1 + j_1] \} \cup \{ \text{wr}[t_1] \} \quad \text{DRF with?} \quad \{ \text{rd}[t_2 + j_2] \} \cup \{ \text{wr}[t_2] \} \]
Splitting protocols

- Syntax-oriented extraction of unsynchronized fragments
- **Compositional** analysis (no data-races between fragments)
- Synchronized loop variables can also be interpreted as a forall-binder
- However, the binder must be shared by both threads (i.e., only one variable shared by both threads)
Conclusion

- Behavioral types being used to enforce data-race freedom
- A compositional analysis, formally proved
- Large experimental evaluation (229 real-world + 258 synthetic = 487 kernels)
- Used our tool to confirm data-races found in the wild
- Our approach is more scalable and more precise (fewer false-positives) than related work
- Source code and proofs available in a free software license

Future directions

- Proving alarms are true (rather than proving false alarms)
- Resource analysis of memory access protocols
- Incompleteness logic to showcase performance bottlenecks

https://gitlab.com/umb-svl/faial
https://gitlab.com/umb-svl/faial-coq